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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/420,798	10/19/1999	YOSHIHIKO IMAMURA	SON-1661	3308

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EXAMINER
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OPIE, GEORGE L

ART UNIT	PAPER NUMBER
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2126

DATE MAILED: 04/07/2004

15

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/420,798

Examiner

George L. Opie

Applicant(s)

Imamura

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**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

**Status**

- 1) ☒ Responsive to communication(s) filed on 3 February 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 23-27, 29-39 and 41-44 is/are pending in the application.
- 4a) Of the above claim(s) ☐ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ☐ is/are allowed.
- 6) ☒ Claim(s) 23-27, 29-39 and 41-44 is/are rejected.
- 7) ☐ Claim(s) ☐ is/are objected to.
- 8) ☐ Claim(s) ☐ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ☐ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on ☐ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☐ All b) ☐ Some \* c) ☐ None of the CERTIFIED copies of the priority documents have been:
1. ☐ received.
2. ☐ received in Application No. (Series Code / Serial Number) ☐.
3. ☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

**Attachment(s)**

- 14) ☐ Notice of References Cited (PTO-892)                      17) ☐ Interview Summary (PTO-413) Paper No(s). ☐.
- 15) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)                      18) ☐ Notice of Informal Patent Application (PTO-152)
- 16) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ☐.                      19) ☐ Other:

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**DETAILED ACTION**

After review and consideration of Applicant's appeal brief and pending claims, this Office Action reopens prosecution of the case.

**1. Request for copy of Applicant's response on floppy disk:**

Please help expedite the prosecution of this application by including, along with your amendment response in paper form, an electronic file copy in WordPerfect, Microsoft Word, or in ASCII text format on a 3½ inch IBM format floppy disk.

Please include all pending claims along with your responsive remarks. Only the paper copy will be entered -- your floppy disk file will be considered a duplicate copy. Signatures are not required on the disk copy. The floppy disk copy is not mandatory; however, it will help expedite the processing of your application. Your cooperation is appreciated.

**2. Claim Rejections - 35 U.S.C. § 112**

3. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 23 recites the phrase "resuming processing of said second user program", but there is no limitation specifying a stop of processing in the second program. This absence of a supporting basis in connection with the "resuming" limitation renders claim 23 vague and indefinite. Claims 25, 27 and 29-35 depend on 23, and are therefore subject to the same rejection.

**4. REQUESTING PRIOR ART REFERRED TO IN THE APPLICATION BUT NOT SUBMITTED**

Applicant gives a discussion of relevant prior art on pages 4-8 of the Application. If applicant is aware of any publications in connection with the referenced prior art, copies are requested so that they may be fully considered.

Applicant is required to respond to this request, failure to do so could result in a NON-RESPONSIVE Office action.

**5. Claim Rejections - 35 U.S.C. § 103**

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The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 23-27, 29-39 and 41-44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the Admitted Prior Art (APA) background of Application.

As to claim 23, the APA teaches a "multiprocessor which is comprised of a plurality of CPUs connected via a common bus and executes a plurality of mutually independent programs in parallel", Application-page3 wherein

a first processor element "processor element 111", page4 of said plurality of processor elements for executing a first user program "instruction codes ... prg A are successively executed", page5 of a plurality of user programs, said first processor element executes a wait instruction, said wait instruction suspends processing of said first user program "when an instruction code 'wait (Prg D)' is executed in the processor element 111, the processing ... enters a synchronization waiting state", page7 and

a second processor element "processor element 114", p7 of said plurality of processor elements for executing a second user program "Prg D" of said plurality of user programs, said second processor element executes a wait release instruction "code 'end' of the subprogram Prg D" said wait release instruction commands said first processor element to resume said processing of said first user program "message indicating the completion of the subprogram Prg D is notified to the processor element 111 . . . As a result, the processor element 111 releases the synchronization waiting state and executes the next instruction code."

Although the APA does not explicitly disclose the first processor executing a "program end instruction" to cause resumption of the second program, it would have been obvious for one skilled in the art, from the APA's "instruction code 'end'" teaching wherein processor 114 conveys a release/resume command to processor 111 when processor 114 has executed an "end" instruction, to provide that the first processor would likewise employ this function to have the second program resume its execution.

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As to claim 24, the APA teaches a first processor element "processor element 111", page4 of said plurality of processor elements for executing a first user program "instruction codes ... prg A are successively executed", page5 of a plurality of user programs, said first processor element executes a wait instruction, said wait instruction suspends processing of said first user program "when an instruction code 'wait (Prg D)' is executed in the processor element 111, the processing ... enters a synchronization waiting state", page7

a second processor element "processor element 114", p7 of said plurality of processor elements for executing a second user program "Prg D" of said plurality of user programs, said second processor element executes a wait release instruction "code 'end' of the subprogram Prg D" said wait release instruction commands said first processor element to resume said processing of said first user program "message indicating the completion of the subprogram Prg D is notified to the processor element 111 . . . As a result, the processor element 111 releases the synchronization waiting state and executes the next instruction code."

As to claim 25, the APA teaches a "multiprocessor which is comprised of a plurality of CPUs" using VLSI *on a single chip for parallel processing*.

As to claim 26, the APA (page 6) teaches the processor executing instructions without suspending program execution after signaling a "release" instruction.

As to claim 27, the APA (page 3) teaches parallel processing programs with "communication between processes" by sending messages over a common bus.

As to claim 29, see the background details on the instruction code "end" executed in the processor elements 111 through 114 on page 7 of the APA.

As to claims 30-31, the APA teaches a first storage means "common memory 15", p4 and second storage means "local memory 32" that correspond to the processing means "processor elements 111 to 114", p5 reading programs from the first storage means "user programs read from the common memory ... and successively supplies instruction codes of the user program stored in the local memory 32 to the processor core 31 for execution.", page 4.

As to claim 32, the APA teaches the system "reads the user programs stored in the common memory 15 into the local memories 32", page 5, until the "end" instruction terminates the process.

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As to claim 33, the APA (pages 5-7) teaches the "wait release" instruction executed by the corresponding processor element as claimed.

As to claim 34, the APA teaches "instruction code 'gen(Prg\_B)' is executed in the processor element 111, . . . Then the subprogram Prb B stored in the common memory 15 is read into the local memory 32 of the processor element 112" pp5-6.

As to claim 35, the APA (page 5) teaches an "arbiter 16" that corresponds to the program execution assigning means and its claimed functions.

As to claims 36-39 and 41-42, note the rejections of claims 23-24, 26, 33 and 35 respectively. Claims 36-39 and 41-42 are the same as claims 23-24, 26, 33 and 35, except claims 36-39 and 41-42 are method claims and claims 23-24, 26, 33 and 35 are apparatus claims.

As to claim 43, see the discussion of claim 23 supra. Claim 43 is functionally equivalent to claim 23, but for the limitation that the other processing means enters a waiting state when executing the release instruction, which would have been an obvious variation from the claim 23 recitations. Having the other processor pause for synchronization when releasing the "wait" of the first process would naturally have flowed from the APA's parallel process coordination teachings.

As to claim 44, note the rejection of claim 26 above. Claim 44 is the same as claim 26, except claim 44 is a computer program product claim and claim 26 is a method claim.

## **7. Response to Applicant's Arguments:**

Applicant argues that the APA does not teach the limitation of a first processor executing a program end serving to resume the processing of a second program. Contrary to Applicant's contention, the APA's teachings clearly meet the limitation of a first processor executing an "end" instruction causing resumption of a second program. The APA specifically describes the claimed coordination of parallel processing, stating "when the last instruction code "end" of the subprogram Prg D is executed in the processor element 114, a message indicating the completion of the subprogram Prg D is notified to the processor element 111 via, for example, the arbiter 16. As a result, the processor element

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111 releases the synchronization waiting state and executes the next instruction code." This disclosure plainly provides the functionality of one processor executing an end that cause resumption of another program. From this, it would have been obvious for one skilled in the art to implement equivalents in corresponding processors to signal a resume to an appropriate coprocessor upon reaching an "end" in the given processor.

Claimed subject matter, not the specification is the measure of the invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art, *In re Self*, 213 USPQ 1,5 (CCPA 1982); *In re Priest*, 199 USPQ 11, 15 (CCPA 1978). The claimed parallel processor elements are clearly subject to a broad interpretation, as detailed in the rejections maintained above. The Examiner has a *duty* and *responsibility* to the public and to Applicant to interpret the claims *as broadly as reasonably possible* during prosecution (see *In re Prater*, 56 CCPA 1381, 415F.2d 1393, 162 USPQ 541 (1969) ).

Applicant's arguments have been fully considered but are deemed to be unpersuasive. For the reasons detailed above, the rejections are maintained as set forth supra.

#### **8. Contact Information:**

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system.

Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see  
<http://pair-direct.uspto.gov>.

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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- ☐ All responses sent by U.S. Mail should be mailed to:

**Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450**

- ☐ Hand-delivered responses should be brought to Crystal Park Two, 2021 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist). All hand-delivered responses will be handled and entered by the docketing personnel. Please do not hand deliver responses directly to the Examiner.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

All OFFICIAL faxes will be handled and entered by the docketing personnel. The date of entry will correspond to the actual FAX reception date unless that date is a Saturday, Sunday, or a Federal Holiday within the District of Columbia, in which case the official date of receipt will be the next business day. The application file will be promptly forwarded to the Examiner unless the application file must be sent to another area of the Office, e.g., Finance Division for fee charging, etc.

- ☐ Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist at **(703) 305-9600**.
- ☐ Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Opie at (703) 308-9120 or via e-mail at *George.Opie@uspto.gov*. Internet e-mail should not be used where sensitive data will be exchanged or where there exists a possibility that sensitive data could be identified unless there is an express waiver of the confidentiality requirements under 35 U.S.C. 122 by the Applicant. Sensitive data includes confidential information related to patent applications.



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